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DATE MAILED: 09/15/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/354,302	Applicant(s) Morzano
	Examiner An T. Luu	Group Art Unit 2816

☒ Responsive to communication(s) filed on *Aug 14, 2000* .

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *three* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1-56 and 82-98* is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-56 and 82-98* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐approved ☐disapproved.

☒ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

Introduction

1. Applicant's response to the restriction filed on 8-14-00 has been received and entered in the case. Applicant elects claims 1-56 and 82-98 (group I) for continued examination, without traverse.

Specification

2. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: the disclosure does not provide or show the limitation "a differential amplifier" to support the recitation of this limitation in claims 9, 21, 34, 38 and 48.

Claim Rejections - 35 USC § 112

3. Claims 9, 10, 15, 16-25, 34, 35 and 38-56 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 9 is unclear since it is not supported by the disclosure. More particularly, there is no disclosure of "differential amplifier" nor structure which meets the recitation of the so-called "differential amplifier" on lines 5-8. The limitation "an

external signal", line 3, is unclear since it is not known if this limitation relates to the limitation "first and second external signals" recited on line 2 of claim 8. The limitation "said input", line 5, does not have a clear an antecedent basis since there is two different "inputs" recited previously.

Claims 21, 34, 38 and 48 have the same problem as that of claim 9. They are rejected for the same reasons set forth above. The merit of claims 9, 21, 34, 38, 48 and their dependent claims 10, 22, 35, 39-47 and 49-56 cannot be determined since Examiner found absolutely no support for claimed inventions as recited in claims.

Claim 15 is rejected for being misdescriptive due to the recitation of phrase "in parallel". There is no two transistors of figures 2 and 3 are "in parallel". By definition in electricity, two devices are in parallel, if and only if, their voltage drops are equal. There is no such thing disclosed in figures.

Claim 16 is rejected for the same reason set forth in claim 15.

Phrase "in parallel" is incorrectly used in claims 13, 25, 37, 47 and 56. These claims are rejected for the same reason set forth in claim 15.

It appears that there is typographical error in claims 31 and 32. They appear depending on claim 28, rather than claim 8. For examination purpose, they are considered to be depended upon claim 28.

Term "gating" recited in claims 13, 25, 37, 47 and 56 is unclear since it does not reflect what is shown in figures. For the purpose of examination, this term is interpreted as "coupling" or "connecting".

Term "gated" recited in claims 3-7, 28-32, 40-44 and 50-54 is unclear since it does not reflect what is shown in figures. For the purpose of examination, this term is also interpreted as "coupling" or "connecting".

Claims 10, 17-20, 22-24, 35, 39-47 and 49-56 are rendered indefinite by the deficiencies of the independent claims noted above.

Claim Rejections - 35 USC § 102

4. Claims 1-3, 6-8, 14-17, 19-20, 26-33, 36, 82-86 and 91-94, to the extent understood in view of the above-noted indefiniteness, are rejected under 35 U.S.C. 102(e) as being anticipated by the Houston et al. reference (U.S. Patent 6,037,808).

The Houston et al. reference discloses in figure 10 an apparatus comprising a first and a second signal input/output lines (at nodes DOUT and /DOUT) for receiving first and a second input signals (DOUT and /DOUT) and transmitting first and second outputs signals (DOUT and /DOUT); and a first and second inverters (T13, T4 and T5,

T14) connected as a latch (output of each inverter is coupled to input of the other) as recited in claim 1.

As to claim 2, figure 1 discloses an enable circuit (T3 and T15) for receiving an enable signal (/SENSE) for enabling or disabling the first and second inverters in response to the enable signal.

As to claims 3 and 6-7, figure 1 shows a first voltage source (Ground) for supplying a first voltage to the first and second inverter via an N-channel transistor T3 responsive to the enable signal SENSE; a second voltage source (Vdd) for supplying a second voltage to the first and second inverter via an P-channel transistor T15 responsive to the inverse of the enable signal (/SENSE). It is inherent that an inverter is needed to inverting the enable signal to achieve its complementary signal.

As to claim 8, elements T3 and T15 are qualified as first, second input buffers wherein SENSE and /SENSE are qualified as first and second external signals as required by claim.

As to claims 14 and 15, barring the term "in parallel", the recitation of these claims read on figure 1 of the cited reference (i.e.,first n- and p-transistors are T4 and T13; second n- and p-transistors are T5 and T14).

As to claim 16, the scope of this claim is similar to the scope of the combination of claims 1, 14 and 15. Thus, it is rejected for the same reasons set for above.

As to claim 17, the scope of this claim is similar to the scope of the combination of claims 1, 2, 14 and 15. Thus, it is rejected for the same reasons set for above.

As to claim 19, the scope of this claim is similar to the scope of the combination of claims 1, 2, 6, 7, 14 and 15. Thus, it is rejected for the same reasons set for above.

As to claim 20, the scope of this claim is similar to the scope of the combination of claims 1, 8, 14 and 15. Thus, it is rejected for the same reasons set for above.

As to claims 26-33 and 36, the scopes of these claims are identical to those of claims 1-8 and 12, respectively. Thus, they are rejected for the same reasons set forth above.

As to claims 82-86 and 91-94, they are rejected as being directed to the method or/and steps derived from the apparatus described in claims 1-3 and 6-8 above.

5. Claims 1 and 11, to the extent understood in view of the above-noted indefiniteness, are rejected under 35 U.S.C. 102(b) as being anticipated by the Oh reference (U.S. Patent 5,838,173).

The Oh reference discloses in figure 2 an apparatus comprising a latch 27 being configured as required by claim 1 and a first (25) and a second (28) driver circuits connecting to the first (A) and second (B) input/output lines, respectively, for boosting the output signal as required by claim 11.

Claim Rejections - 35 USC § 103

6. Claims 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Houston et al. reference (U.S. Patent 6,037,808).

The Houston reference discloses all the limitation required by claims 4-5 except for showing a proper type of transistors (i.e., n- and p-type transistors) connected to the first and second voltage sources. It is notoriously well-known in the art that N- and P-type transistors are complementary transistors and they can be used interchangeably. Thus, it would have been obvious for one skilled in the art to use either type of transistor in his circuit since the selection between complementary transistors is seen as design expedient dependent upon the particular of the application.

7. Claims 12 and 13, to the extent understood in view of the above-noted indefiniteness, are rejected under 35 U.S.C. 103(a) as being unpatentable over the Oh

reference (U.S. Patent 5,838,173) in view of the Garcia reference (U.S. Patent 5,949,259).

The Oh reference discloses all the claimed limitations recited in claims 12 and 13 including a driver circuit. The Oh reference does not disclose a specific structure of the driver circuit as recited in claims. The Garcia reference discloses in figure 6 a driver circuit comprising at least a first and a second driver inverter (202; P4 and N4) connected in series; and a third inverter (P2,N3) wherein the third inverter and the series connected inverters have the same input and the output of the third inverter connected to a device N1 such that the output of the series connected inverters is set to a predetermined voltage as understood by claim 13 based on figure 5 of the instant application. It would have been obvious for one skilled in the art to replace a generic driver circuit taught by Oh with the one taught by Garcia because the skilled artisans will easily recognize that a driver circuit can be implemented in many different ways in the art, one of such way is as shown in the Garcia for controlling a slew-rate of an output buffer circuit.

8. Claims 18, 23-25, 87-90 and 95-98 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Houston et al. reference (U.S. Patent 6,037,808) as applied to

claims 1-3, 6-8 and 14-15 above, in view of the Oh reference (U.S. Patent 5,838,173) and further in view of the Garcia reference (U.S. Patent 5,949,259).

As to claim 18, the scope of this claim is similar to the scope of the combination of claims 1, 2, 3, 4, 5, 14 and 15. Thus, it is rejected for the same reasons set forth above.

As to claim 23, the scope of this claim is similar to the scope of the combination of claims 1, 11, 14, 15 and 16. Thus, it is rejected for the same reasons set for above.

As to claim 24, the scope of this claim is similar to the scope of the combination of claims 1, 11, 12, 14, 15 and 16. Thus, it is rejected for the same reasons set for above.

As to claim 25, the scope of this claim is similar to the scope of the combination of claims 1, 11, 12, 13, 14, 15 and 16. Thus, it is rejected for the same reasons set for above.

As to claim 87-90 and 95-98, it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. *Ex parte Masham*, 2 USPQ2d 1647 (1987).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. (See enclosed Form PTO-892).

10. Any inquiry concerning this communication should be directed to An T. Luu whose phone number is (703)-308-4922 and facsimile number is (703)-308-7722.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reach on (703) 308-4876. The fax phone number for this Group is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application should be directed to group receptionist at (703)-308-0956.

9/6/00

An T. Luu

AU 2816